WHAT IS CLAIMED IS:

1. A process for determining the optimum load driving capacity for a driving node in a logic circuit comprising the steps of:

A) extracting the logic equations of the logic circuit from a circuit description thereof;

B) analyzing the fan-out of the driving node to determine if the total number of pass transistor loads is excessive compared to a predetermined driving capacity;

C) if, during step B), it is determined that the total number of pass transistor loads is exceeds an absolute maximum, then:

1) to the logic equations of the logic circuit, adding logic equations which represent the sum of the pass transistor loads;

2) to the logic equations of the logic circuit, adding comparator logic equations to compare the number of pass transistors turned on from one to the absolute maximum;

3) using a formal proof program to analyze the logic circuit and determine which of the comparators have a true output;

4) identifying the comparator for the largest number which has a possible true output to determine the highest possible actual load; and

5) if necessary, adjusting the driving capacity of the driving node to handle the determined highest possible actual load.

2. A process for determining the optimum load driving capacity for each driving node in a complex logic circuit comprising the steps of:

A) extracting the logic equations of the logic circuit from a circuit description thereof;

B) analyzing the fan-out of each driving node to determine if the total number of pass transistor loads of the analyzed node is excessive compared to a predetermined driving capacity;

C) for each driving node flagged during step B:

1) to the logic equations of the logic circuit, adding logic equations which represent the sum of the driving node's pass transistor loads; and

2) to the logic equations of the logic circuit, adding comparator logic equations to compare the number of pass transistors turned on from one to the absolute maximum for the driving node;

D) using a formal proof program to analyze the logic circuit and determine which of the comparators have a true output;

E) for each flagged driving node:

1) identifying the comparator for the largest number which has a possible true output to determine the highest possible actual load for the driving node; and

2) if necessary, adjusting the driving capacity of the driving node to handle the determined highest possible actual load.

3. A process for determining the required load driving capacity for a driving node in a logic circuit comprising the steps:

A) obtain a logical description of an electronic circuit;

B) identify logic nodes for further analysis within the circuit which are driven by gates that have variable loading dependent on the logical state of the logic circuit during operation;

C) develop added logical equations which describe arithmetically the loading on the driving gate as it depends on the logical value of other nodes in the logic circuit; and

D) use a program which implements formal mathematical methods of logical proof to determine the largest driving capacity required of the driving node by examining the outputs of the equations added to the logic to determine the largest actual loading that can be logically

placed upon the driving gate with consideration as to the possible overall logical state of the logic circuit.

4. The process of Claim 3 wherein the logical description of the electronic circuit is developed by a program that extracts the logical description from an electronic description of the circuit describing the interconnection of transistors and other electronic elements.

5. The process of Claim 4 including the added step in which the electronic circuit is modified to adjust the driving capacity of at least one node based upon the results of the formal proof process.

6. The process of Claim 3 wherein the added logic equations utilize integer values for specifying and calculating the loading.

7. The process of Claim 4 wherein the added logic equations utilize integer values for specifying and calculating the loading.

8. The process of Claim 5 wherein the added logic equations utilize integer values for specifying and calculating the loading.

9. The process of Claim 3 in which that analysis of logic nodes is further restricted to only those nodes identified in preliminary analysis as being in

violation of requirements based upon absolute worst case loading without consideration as to the logical state of the logic circuit.